Amendments To The Claims

1.(currently amended) A printer, comprising:

~~(a)~~ a first virtual memory address bus;

a plurality of bus masters comprising a central processing unit, an input/output port and a print engine interface coupled to the first address bus;

~~(b)~~ a second physical memory address bus;

a printer memory coupled to the second address bus; and

~~(c)~~ an address translation unit ~~(ATU),~~ coupled to the first and second address buses, the address translation unit operable to translate virtual addresses received from ~~at least two~~ the bus masters over ~~connected to~~ the first bus into physical memory addresses.

2.(currently amended) The printer of claim 1, wherein the address translation unit ~~ATU~~ is further operable to transmit ~~the~~ physical memory addresses ~~address~~ over the second bus.

3. (currently amended) The printer of claim 2, wherein one of the bus masters comprises a direct memory access controller associated with a print engine interface, and the printer further comprising: ~~(d)~~ a print engine coupled to the print engine interface ~~first address bus~~.

4. (currently amended) The printer of claim 3, wherein one of the bus masters comprises the ~~further comprising: (e) a~~ central processing unit ~~(CPU)~~ coupled to the first address bus.

5. (currently amended) The printer of claim 4, wherein another of the bus masters comprises ~~further comprising: (f)~~ a direct memory access ~~DMA~~ controller associated with the input/output port coupled to the first address bus.

6-7.(cancelled)

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8.(currently amended) The printer of claim 1 ~~7~~, wherein the address translation unit ~~ATU~~ is operable to translate ~~the~~ virtual addresses received over the first address bus ~~from the CPU controller and the DMA controller~~ into physical addresses for addressing the printer memory and to then transmit these physical addresses to the memory over the second address bus.

9-20.(cancelled)

21.(new) A printer, comprising:

a first virtual memory address bus;

a second physical memory address bus;

a central processing unit coupled to the first address bus;

an input/output port having a first direct memory access controller coupled to the first address bus, the first direct memory access controller operable to manipulate data using virtual memory addresses;

a print engine interface having a second direct memory access controller coupled to the first address bus, the second direct memory access controller operable to manipulate data using virtual memory addresses;

a print engine coupled to the print engine interface;

a printer memory coupled to the second address bus, the memory operable to store data using physical memory addresses; and

an address translation unit coupled between the first address bus and to the second address bus, the address translation unit operable to translate between virtual memory addresses and physical memory addresses.

22.(new) The printer of claim 21, wherein:

the address translation unit includes a translation table mapping virtual memory addresses to corresponding physical memory addresses; and

the printer memory comprises read only memory storing a translator program that when executed by the central processing unit maintains the translation table.

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23.(new) A printer, comprising:

a central processing unit, an input/output port and a print engine interface operable in a virtual memory address space;

a memory operable in a physical memory address space; and

a translator operatively coupled between the memory and the central processing unit, input/output port and print engine interface, the translator operable to translate virtual memory addresses from the virtual memory address space into physical memory addresses for the physical memory address space.

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